# LOW-POWER CONTENT ADDRESSABLE MEMORY CELL

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ABSTRACT OF THE DISCLOSURE

A content addressable memory (CAM) cell that includes a static random access memory (SRAM) cell that operates in response to a $V_{CC}$ supply voltage. A first set of bit lines coupled to the SRAM cell are used to transfer data values to and from the SRAM cell. The signals transmitted on the first set of bit lines have a signal swing equal to the $V_{CC}$ supply voltage. A second set of bit lines is coupled to receive a comparison data value. The signals transmitted on the second set of bit lines have a signal swing that is less than the $V_{CC}$ supply voltage. For example, the signal swing on the second set of bit lines can be as low as two transistor threshold voltages. The second set of bit lines is biased with a supply voltage that is less than the $V_{CC}$ supply voltage. A sensor circuit is provided for comparing the data value stored in the CAM cell with the comparison data value. The sensor circuit pre-charges a match sense line prior to a compare operation. If the data value stored in the CAM cell does not match the comparison data value, the match sense line is pulled down. The signal swing of the match sense line is smaller than the $V_{CC}$ supply voltage. For example, the signal swing on the match sense line can be as low as one transistor threshold voltage.